

WEST Search History

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DATE: Monday, October 04, 2010

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
<i>Interference</i>			
<i>DB=PGPB; PLUR=YES; OP=OR</i>			
<input type="checkbox"/>	L16	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1 and fetch \$ 3 and head and tail and de \$ queue \$ 3 and memory and response and return \$ 3 and en \$ queue \$ 3).clm.	1
<input type="checkbox"/>	L15	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1 and fetch \$ 3 and head and tail and de \$ queue \$ 3 and memory and response).clm.	1
<input type="checkbox"/>	L14	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1 and fetch \$ 3 and head and tail and de \$ queue \$ 3).clm.	1
<input type="checkbox"/>	L13	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1 and fetch \$ 3 and head and tail).clm.	1
<input type="checkbox"/>	L12	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1 and fetch \$ 3 and head).clm.	1
<input type="checkbox"/>	L11	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1 and fetch \$ 3).clm.	1
<input type="checkbox"/>	L10	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3 and command \$ 1).clm.	1
<input type="checkbox"/>	L9	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1 and de \$ queue \$ 3).clm.	1
<input type="checkbox"/>	L8	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1 and descriptor \$ 1).clm.	1
<input type="checkbox"/>	L7	(cache and processor \$ 1 and element \$ 1 and queue \$ 3 and tail and head and pointer \$ 1).clm.	2
<input type="checkbox"/>	L6	(memory and queue \$ 3 and descriptor \$ 1 and pointer \$ 3 and head and tail \$ 1 and count \$ 1 and (modify \$ 3 or updat \$ 3) and cache and processor \$ 1).clm.	0
<input type="checkbox"/>	L5	(memory and queue \$ 3 and descriptor \$ 1 and pointer \$ 3 and head and tail \$ 1 and count \$ 1 and (modify \$ 3 or updat \$ 3)).clm.	2
<input type="checkbox"/>	L4	(memory and queue \$ 3 and descriptor \$ 1 and pointer \$ 3 and head and tail \$ 1 and count \$ 1).clm.	3
<input type="checkbox"/>	L3	(memory and queue \$ 3 and descriptor \$ 1 and pointer \$ 3 and head and tail \$ 1 and count \$ 1 and element \$ 1).clm.	0
(memory and queue \$ 3 and descriptor \$ 1 and pointer \$ 3 and head and tail \$			

□	L2	1).clm.	13
□	L1	(memory and queue \$ 3 and descriptor \$ 1 and pointer \$ 3).clm.	75

END OF SEARCH HISTORY